**Claims:**

Please cancel claims 44-65. The claims are as follows:

1. (Canceled)

2. (Previously Presented) The method of claim 5, wherein said second width has a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

3. (Previously Presented) The method of claim 5, further including removing said patterned hard mask layer.

4. (Previously Presented) The method of claim 5, wherein said patterned hard mask layer comprises silicon oxide.

5. (Previously Presented) A method of fabricating a polysilicon line, comprising:

forming a patterned hard mask layer over a polysilicon layer;

patterning the polysilicon layer to provide a hard mask-capped polysilicon line having a first width; and

isotropically removing portions of said polysilicon line to reduce said polysilicon line to a second width by converting a surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer.



PAGE 3/9 * RCVD AT 11/23/2004 12:03:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-06

6. (Previously Presented) The method of claim 5, wherein the step of removing portions of the polysilicon line includes oxidizing a surface of said polysilicon line in a saturated aqueous solution of $O_3$ to form said oxide layer on said polysilicon line followed by etching said oxide layer in a solution comprising HF in water.

7. (Previously Presented) The method of claim 5, wherein the step of removing portions of the polysilicon line includes oxidizing a surface of said polysilicon line in a saturated aqueous solution of $O_3$ to form said oxide layer on said polysilicon line followed by etching said oxide layer in an HF containing vapor.

8-18. (Canceled)

19. (Previously Presented) A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width;

isotropically removing portions of the polysilicon electrode to reduce said polysilicon line to a second width by converting a surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer; and

removing said patterned hard mask layer.



PAGE 4/9 * RCVD AT 11/23/2004 12:03:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-06

20. (Previously Presented) The method of claim 19, wherein said second width has a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

21. (Canceled)

22. (Previously Presented) The method of claim 19, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon electrode and said patterned hard mask.

23. (Original) The method of claim 19, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

24. (Previously Presented) The method of claim 19, wherein said substrate is selected from the group consisting of silicon substrates, silicon on insulator substrates, gallium arsenide substrates and sapphire substrates.

25. (Previously Presented) The method of claim 19, wherein the step of removing portions of the polysilicon electrode includes oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of $O_3$ to form said oxide layer on said polysilicon electrode followed by etching said oxide layer in a solution comprising HF in water.



PAGE 5/9 * RCVD AT 11/23/2004 12:03:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-06

26. (Previously Presented) The method of claim 19, wherein the step of removing portions of the polysilicon electrode includes oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of $O_3$ to form said oxide layer on said polysilicon electrode followed by etching said oxide layer in an HF containing vapor.

27. (Canceled)

28. (Canceled)

29. (Previously Presented) A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width;

measuring said first width;

comparing said first width to a target width and determining a differential between said first width and said target width;

calculating a number of polysilicon oxidation/isotropic polysilicon oxide etch cycles based on said differential; and

performing the calculated number of polysilicon oxidation/isotropic polysilicon oxide etch cycles.



PAGE 6/9 * RCVD AT 11/23/2004 12:03:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-06

30. (Previously Presented) The method of claim 29, wherein said target width has a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

31. (Original) The method of claim 29, further including removing said patterned hard mask layer.

32. (Previously Presented) The method of claim 29, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon electrode and said patterned hard mask.

33. (Original) The method of claim 29, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

34. (Previously Presented) The method of claim 29, wherein said substrate is selected from the group consisting of silicon substrates, silicon on insulator substrates, gallium arsenide substrates and sapphire substrates.

44–65. (Canceled)



PAGE 7/9 * RCVD AT 11/23/2004 12:03:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-06